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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/889,558	07/27/2001	Charles Leroux		7670

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/889,558	LEROUX, CHARLES	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/17/03 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 11, 12, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by DE 31 42 591 to Turley et al.

Regarding the claims, Turley discloses a plurality of Zener diodes mounted in series (figures 6 and 7, formed from 69-75) formed in a semiconducting layer (68) of an SOI substrate, the semiconducting layer covering an insulating layer (66; see figure 7), and having two regions of heavily doped opposite conductivity types extending to the insulating layer (figure 7); and a contact pin 51) connected to the electronic component (MOSFET 52) and connected through the Zener diodes to ground (through 60; figure 5).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turley et al. in view of U.S. Patent No. 5,736,779 to Kobayashi.

Regarding claim 13, Turley fails to disclose that the Zener diode is formed by two regions of heavily doped opposite conductivity types separated by a region doped to an average level.

Kobayashi discloses a silicon on insulator Zener diode chain having heavily doped n and p regions separated by an average doped p region (figure 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the diode structure of Turley such that an average doping level region is formed between two heavily doped regions, as taught by Kobayashi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a Zener diode having an average-doping level region between two heavily doped regions, in order to prevent leakage currents in the Zener diode and allow for the easy control and selection of the Zener voltage (see Kobayashi, figure 8; column 3, lines 45-55).

Regarding claim 13, neither Turley nor Kobayashi specify the doping concentration levels for the Zener diode, but Kobayashi does disclose that the implant dose is high (see Kobayashi, column 6, lines 30-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the concentration for the heavily doped layer is on the order of 1E20 atoms/cm3 and the concentration of the average level is 1E18 atoms/cm3 in the invention of Turley as modified by Kobayashi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to specify a such concentrations, because Kobayashi teaches that the impurity concentration levels are selected in order to achieve the required Zener voltage for protecting the device (Kobayashi, column 2, lines 55-61). Although neither Turley nor Kobayashi specify the exact doping levels for the Zener diode, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

6. Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,708,288 to Quigley et al. in view of U.S. Patent No. 5,536,958 to Shen et al.

Regarding claims 11, 12, and 15, Quigley discloses a protection device comprising: a Zener diode (36; 242, 244, 246) formed in a semiconducting layer (130) of a SOI substrate (column 4, lines 23-50), the semiconducting layer covering an insulating layer (110) and having two regions of heavily doped opposite conductivity types (242, 246) extending to the insulating

layer (figure 3); and a contact pin connected to the component and through the Zener diode to ground (figure 1).

Quigley fails to disclose that a plurality of Zener diodes mounted in series.

Shen discloses a plurality of Zener diodes mounted in series (figures 2 and 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the protection structure of Quigley, such that in place of the single Zener diode of Quigley, a plurality of Zener diodes mounted in a series is used, as suggested by Shen. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a plurality of Zener diodes, because by adjusting the number of diodes formed in the diode chain, the amount of voltage protection applied to the electronic component can be selected such that an appropriate value is used for the device-to-be protected (see Shen, column 4, lines 8-12).

Regarding claim 13, Quigley discloses a region doped to an average level (244) between the two highly doped regions (242 and 246).

Regarding claim 14, Quigley discloses that the implant dose for the heavily doped regions is very high (column 5, lines 35-60) and that the dose for the average doped region is reasonably low (column 5, lines 25-34), but fails to specify the exact concentration resulting from such dosages.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the concentrations of the Zener regions of Quigley as modified by Shen are on the order of 1E20 atoms/cm3 and 1E18 atoms/cm3. The rationale is as follows: A person having ordinary skill in the art would have been motivated to specify the doping concentrations supra, because Quigley teaches that the heavily doped regions are implanted with a high dosage,

which would result in a very high level of doping (see Quigley, column 5). Also, by adjusting the concentration of each region, the desired Zener voltage can be achieved to adequately protect the electronic component. Although Quigley does not specify the exact concentration, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Regarding claims 16 and 17, Quigley discloses that the Zener diode is connected to other components in the IC using a silicide and/or a metallization (column 4, line 50-column 5, line 14).

Quigley fails to teach that the plurality of Zener diodes are interconnected using silicide or a metallization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the diode chain of Quigley as modified by Shen, such that the Zener diodes in the chain are connected through a metallization or silicide layer. The rationale is as follows: A person having ordinary skill in the art would have been motivated to connect the Zener diodes using a metallization or a silicide, because Quigley shows that silicide and metal traces are commonly used and suitable for interconnecting IC components including Zener diode components (see Quigley, column 4, line 50 – column 5, line 14). A person skilled in the art would further appreciate that by connecting the Zener diodes using a silicide or metallization, rather than using a back-to-back structure, greater flexibility for laying out the IC design can be achieved.

Response to Arguments

7. Applicant's arguments with respect to claims 11-17 have been considered but are moot in view of the new grounds of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,365,099 to Phipps et al. discloses a Zener diode chain disposed on an insulator for ESD protection.

b. IEEE article to Cohen et al discloses a comparison of various ESD protection circuits for SOI-type devices.

c. U.S. Patent No. 5,610,790 to Staab et al. discloses various ESD protection circuits for use with SOI devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800